ABSTRACT OF THE DISCLOSURE

Disclosed are a vertical MOS transistor which lowers the gate resistance, improves the high frequency characteristics, and improves the yield compared with a conventional one and a method of manufacturing the same. When gate voltage is applied to a gate electrode, a channel is formed in a body region along a trench , and electrons or current flow(s) from a drain layer to a source layer. Here, a gate in the trench has a laminated structure of a polycrystalline silicon film and a metal silicide.. Therefore, a gate resistance is lowered and the high frequency characteristics are improved. Further, according to the structure and the method of manufacturing, a concave portion generated at an upper portion of the gate in the trench when etching for forming the gate is less liable to be generated, and thus, malfunction and insufficient reliability due to the concave portion can be avoided.